ABSTRACT

A system and method for decreasing the memory access time by determining if data will be written directly to the array or be posted through a data buffer on a per command basis is disclosed. A memory controller determines if data to be written to a memory array, such as a DRAM array, is either written directly to the array or posted through a data buffer on a per command basis. If the controller determines that a write command is going to be followed by another write command, the data associated with the first write command will be written directly into the memory array without posting the data in the buffer. If the controller determines that a write command will be followed by a read command, the data associated with the write command will be posted in the data buffer, allowing the read command to occur with minimal delay, and the posted data will then be written into the array when the internal I/O lines are no longer being used to execute the read command.